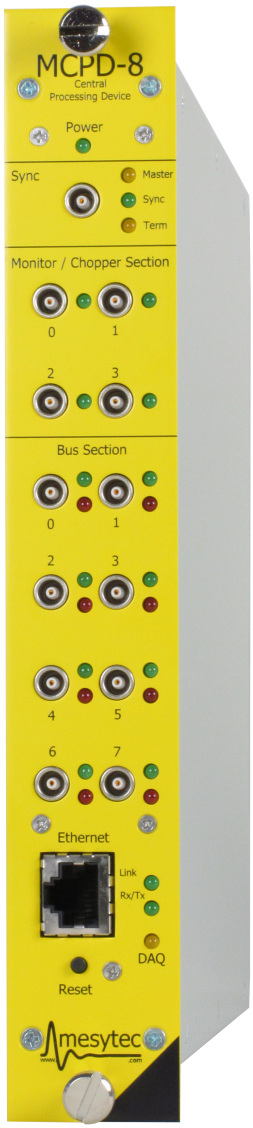
MCPD-8 is a module which collects the data of up to eight MPSD-8+ or MSTD-16 modules, creates a full time stamp with 48bits width, buffers the position amplitude and timing data and sends it via ethernet to a data acquisition PC.
It also transmits the configuration data between control PC and the peripheral modules. There is a communication path via synchronisation line to the other MCPD-8 or MDLL modules in a setup, allowing to synchronise the time stamps between those data collectors, and transmit basic commands like start, stop and run number.

Features:



- **High rate capability** up to 2 mega events/s permanently. No additional dead time up to the rate limit. Bursts with rates up to 6.4 mega events/s can be stored in the main buffer.
- **48 bit time stamp** for all events with 100ns resolution (running 325 days).
- **6 external digital inputs** for connection of monitor counters or chopper signals. Can create fully time stamped events of multiple types which are fed to the event data stream.
- **2 voltage inputs** digitized by 12bit ADCs, sample rate max. 100kHz. Data can be time stamped and sent to the data stream
- **2 voltage outputs**, voltage created by 12bit DACs. Can be controlled via control PC.
- **2 digital outputs**, controlled by PC
- **Synchronisation bus,** is a Lemo coax connection between several MCPD-8 or MDLL modules. One MCPD-8 module is configured as master module and synchronises all connected modules. Also basic signals like start, stop and a run number is transmitted.
  The master MCPD-8 itself can be synchronised to an externally applied 10 MHz clock (i.e. chopper time base)
- **PC Software:** MCPD-8 and MDLL communicate with the control and (if existing separately) data acquisition PCs using a UDP based protocol. The open source data acquisition and control software **mesydaq/ qmesydaq,** running on Linux OS, is provided for data acquisition, online visualisation and system control.

mesytec GmbH & Co. KG
Wernher-von-Braun-Str. 1, D-85640 Putzbrunn, Germany
phone: +49 - 89 / 456007-30 fax: +49 - 89 / 456007-39
info@mesytec.com - www.mesytec.com

Functional Overview

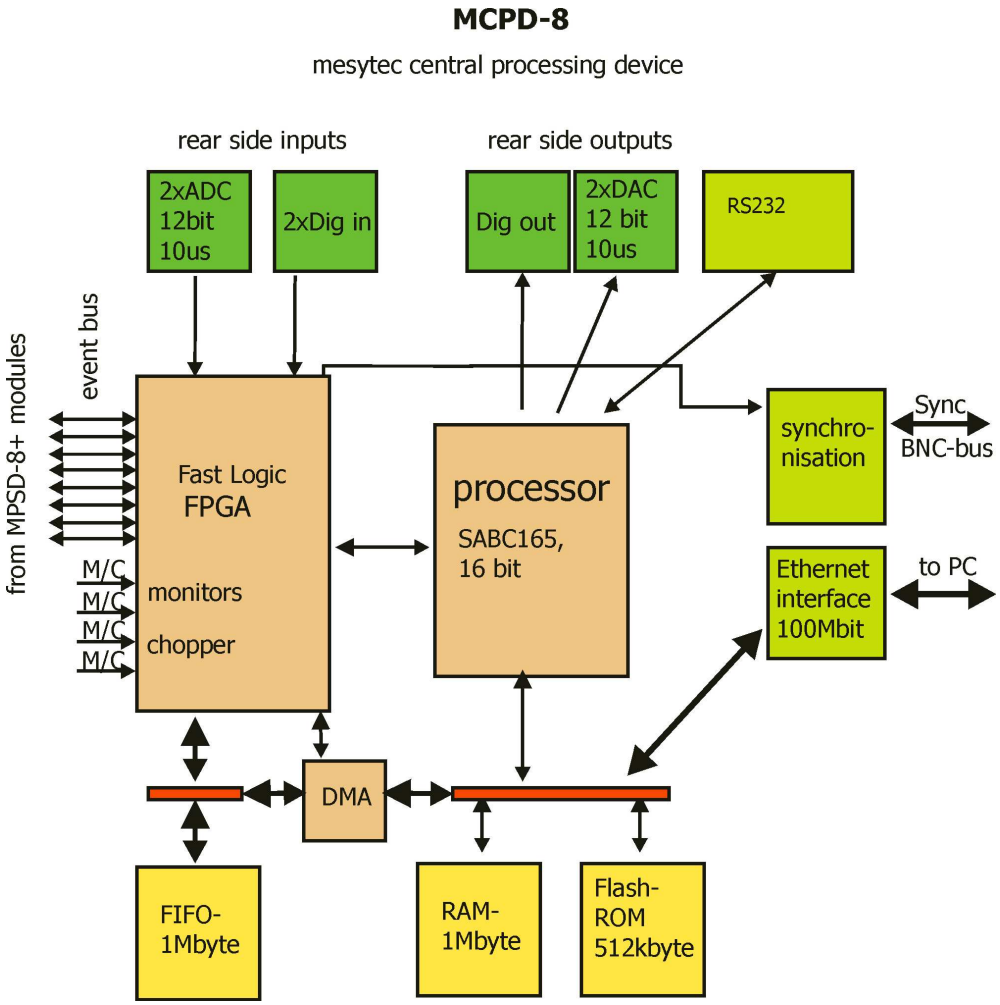
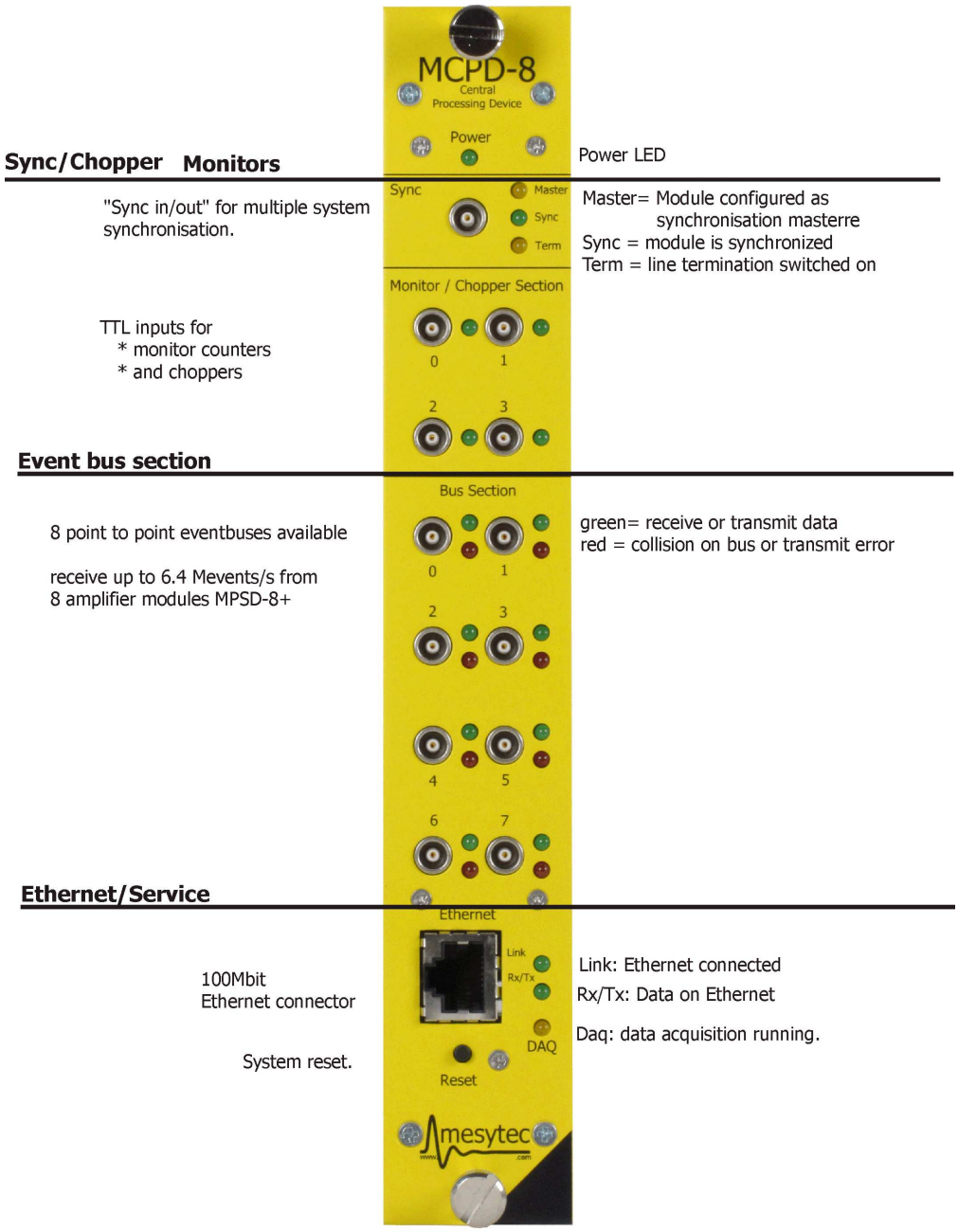


fig. 5 : internal design of the MCPD-8 module

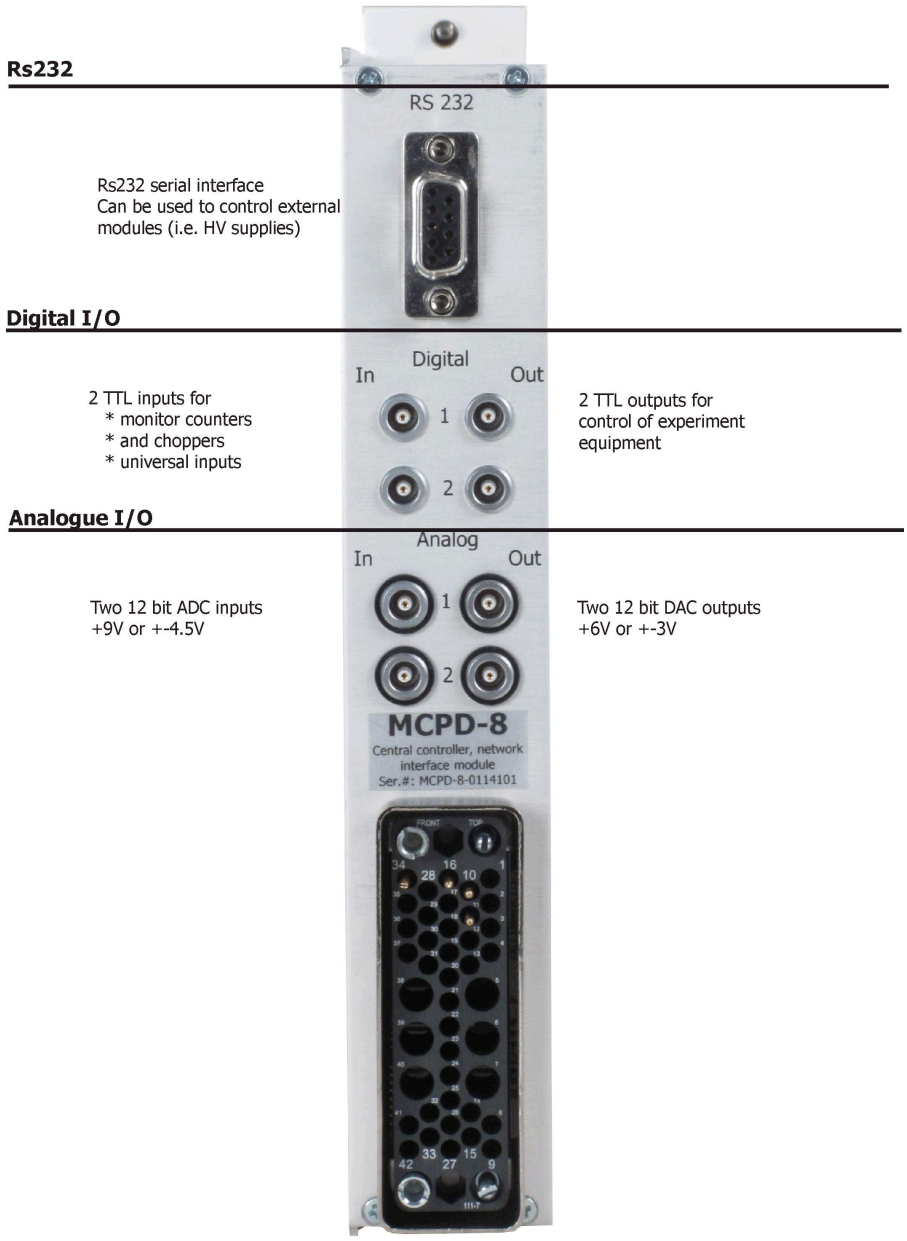
The internal design mainly consists of two blocks.:
The first is a programmable logic, which services the eight fast event buses, creates the time stamps, accumulates all incoming data in a 1Mbyte FIFO (= 128kevents), and counts the external monitor signals. As additional features the MCPD-8 has two ADC inputs (12 bit) and can create periodic time stamped ADC events which are accumulated with the other events in the FIFO. This is for example useful to add additional experiment parameters (temp, pressure, fields, …) to the data stream.
The programmable logic does not add any additional dead time to the event bus. It can manage event bus rates of up to 6.4MHz.

The second block is a fast 16bit microprocessor which delivers an additional buffer of up to 1Mbyte and services the ethernet connection. It can deliver the theoretical maximum transmission data rate of the 100Mbit on ethernet. This is possible due to a fast DMA unit which directly dumps the list mode data from FIFO to the ethernet controller without stopping the data accumulation. The maximum event transmission rate to the ethernet will be around 2Mevents/s.
(6bytes per event: 10bit amplitude, 10bit position and time stamp + 5% protocol overhead)
A system with 128 detector tubes (16 x MPSD-8, 2 x MCPD-8) will process a peak rate of 12.8MHz (detector limit100 kHz per detector) and an average rate of 4MHz.

Front panel elements



Rear panel elements



MCPD-8 data sheet

Power consumption:

- P = 4W
- U = +6V, 0.70A (with oven stabilized quartz: up to 1A for 10s at power up)
  = -6V, 0.02A
  = +12V, 0.1A (optional: for DAC output only)

Event buses:

- Maximum event bus data rate: up to 0.8MHz / bus
- Event bus dead time per event: down to 1.2us
- Signal level: 0 to +0.7V; Terminated inputs.

Ethernet:

- 100Base-TX
- Maximum Ethernet event rate to PC: 2MHz

6 Monitor, chopper inputs:

- TTL input:
- minimum High level 2.8V
- maximum low level: 0.8V
- Minimum pulse length: 200ns

2 Digital outputs:

- 5V level, max. 10mA

2 DAC outputs:

- 0 to 6V or ± 3V, (selected by jumpers)
  max 30mA, protected

2 ADC inputs:

- 0 to 9V or ± 4.5V (selected by jumpers)
  input resistance 6kΩ

Sync in / out:

- Provides and receives time reference and control signals
- Oscillator: 1.25MHz (is multiplied by 8 in the receiver modules)

Time stamp generation:

- Standard oscillator: stability 10^{-5}
- **Option:** Oven stabilized oscillator: stability 10^{-7}