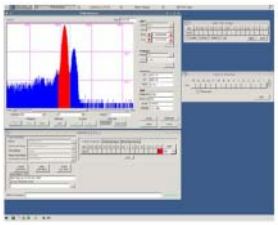
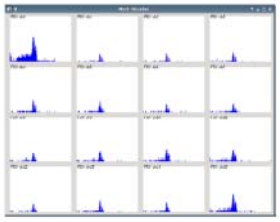
NKI GLASS CO.,LTD

LIST MODULE SERISE
A3XXX

A3200 QDC
A3300 TDC
A3400 ADC

•A3XXX is multi-input modules of the VME standard.
• All modules are designed in the concept that it unified, and be superior in affinity.
•The 200MHz clock had built-in can provide a time stamp of minimum 5ns.
•Each board has 16 input and gates. They operate for independence.
•Can use common gate & VETO of the board unit.
•A3XXX can do the PHA measurement with the LIST measurement.
•Can synchronize with a clock of several A3XXX.
•A24/34,D16/D32/BLI Data transfer , MCST





3000-E-C / SVP-511

Can give the control program for A3XXX on the basis of LINUX.
Can do control in the Ethernet by VME-PC based on the PowerPC in the latest system.
All the data are stored with a text on PC.
You can easily access your data.
The program is common to all A3XXX.
You do not have to change a program every purpose.

•This product is developed for the purpose of using it in Japan.
•When you plan use except Japan, The duty in accordance with the law of the countries concerned government produces you.

Please perform an inquiry of more information at the following.

NIKIGLASS CO.,LTD.
9-7 Mita 3-chome,Minato-ku,Tokyo 108-0073,JAPAN
Email to : sales@nikiglass.com

	A3200 QDC	A3300 TDC	A3400 PDC
Number of inputs/ board	16(LEMO)		
Compliance voltage of input signal	0 ～ - 2.5V		
Start/Stop input		Fast Neg.NIM logic 50Ω tw:≧10ns	
Input signal			0～+10V POS UNI. Min rise time : 200ns ,mix width 500ns 1kΩ
Dynamic range	0 ～ 2000pC		
Full scale		100ns/200ns/400ns/800ns/1600ns	
Resolution	13bits(250fC/count)	13bits(12.5ps/25ps/50ps/100ps/200ps)	
Conversion gain	8k/4k/2k/1k/512/256 Independent every inputs		
Conversion time	≦400ns/ch(6.4us/all channel)		
Integral non- linearity	≦±0.1%(5-95% of full scale)		
Differencial non-linearity	≦±1%(5-95% of full scale)		
Throughput	Max 2.5Mcps/board MAX 1Mcpa (single input)		
ZERO ADJUST			12bits ±5% of full scale
LLD			12bits ±10% of full scale
Operation mode	PHA/Free Run List /Triggered List		PHA/Gated List/Free Run List /Triggered List
Data memory	256kX32bits Dual port memory PHA : 8kx32bits x 16inputs LIST : 127kx32bits ring buffer Register : 1kx32bits		
Preset time for PHA	Real/Live/ROI Integral/ROI peak		
Event counter	28bits		
Time stump	40bits ,5ns/10ns/20ns/50ns/100ns/200ns/500ns/1us clock selectable		
Independent gate inputs	tw:≧10ns,Fast Neg.NIM 50Ω,Delay time :max 30ns		tw:≧200ns-10us,Fast Neg.NIM 50Ω,Delay time :max 30ns
Common gate input	tw:≧20ns-1us,Fast Neg.NIM 50Ω,Delay time :max 30ns		tw:≧200ns-10us,Fast Neg.NIM 50Ω,Delay time :max 30ns
Common start/stop		tw:≧10ns,Fast Neg.NIM 50Ω,Delay time :max 30ns	
Common gate counter			32bits
Fast Clear input	tw:≧10ns,Fast Neg.NIM 50Ω		
Fast Clear time	≦400ns		
VETO Input	tw:≧10ns,Fast Neg.NIM		
Busy output	TTL		
Clock synchronization	ATICbus		
VME bus interface	A24/32 addressing,D16/32/BLT Data transfer, MCST equivalence		
Power	+5 , -12V , +12V		